AMENDMENTS TO THE CLAIMS:

Non-elected claims 7-16 are canceled without prejudice or disclaimer.

1. (Currently amended) A method of producing a layout pattern of a semiconductor device, comprising ~~the steps of~~:

arranging primitive cells including ~~having~~ circuit patterns of constituent elements of said semiconductor device in an element formation area of said semiconductor device; and

arranging at least one fill cell including ~~with~~ a diffusion layer and no wiring, in a vacant area in the element formation area of said semiconductor device that is generated after said primitive cells associated with all constituent elements of said semiconductor device have been arranged.

2. (Original) A method according to claim 1, wherein said fill cells are arranged such that said diffusion layers are uniformly distributed in said element formation area of said semiconductor device.

3. (Currently amended) A method according to claim 1, wherein said fill cells are arranged such that a distribution ratio of said diffusion layers falls within a ~~the~~ range of 30 - 55% of ~~in~~ said element formation area, said distribution ratio being a ~~the~~ proportion of said diffusion layers that are distributed in said element formation area of said semiconductor device.

4. (Original) A method according to claim 1, wherein a plurality of types of fill cells having different sizes that are each identified by an identifier having the same amount of information are prepared and are arranged in said vacant area in order of size starting from the largest fill cells that can be arranged in said vacant area.

5. (Original) A method according to claim 1, wherein said constituent elements are grouped such that constituent elements having related operation are sorted into the same group; and

said primitive cells associated with constituent elements that belong to the same group are arranged in proximity.

6. (Currently amended) A method according to claim 1, further comprising: ~~a step of~~ producing mask data for fabricating a reticle to be used in fabricating said semiconductor device, from a layout pattern in which said primitive cells and said fill cells are arranged.

7-16. (Canceled).

17. (New) A method according to claim 1, further comprising:

combining a plurality of fill cells to form at least one composite fill cell having a predetermined size;

detecting vacant areas in the element formation area of said semiconductor device after said primitive cells associated with all constituent elements of said semiconductor device have been arranged;

detecting a continuous vacant area which includes a same size as said predetermined size of said composite fill cell;

arranging said composite fill cell in said continuous vacant area.

18. (New) A method according to claim 17, further comprising:

arranging at least one fill cell in a remaining vacant area of said vacant areas after said composite fill cell is arranged.

19. (New) A method of producing a layout pattern of a semiconductor device, comprising:

arranging primitive cells including circuit patterns of constituent elements of said semiconductor device in an element formation area of said semiconductor device;

detecting vacant areas in the element formation area of said semiconductor device after said primitive cells associated with all constituent elements of said semiconductor device have been arranged; and

arranging at least one fill cell, which includes a diffusion layer and no wiring, in one of said detected vacant areas in the element formation area of said semiconductor device.

20. (New) A method according to claim 19, wherein said fill cells are arranged such that said diffusion layers are uniformly distributed in said element formation area of said semiconductor device.

21. (New) A method according to claim 19, wherein said fill cells are arranged such that a distribution ratio of said diffusion layers falls within a range of 30 - 55% of said element formation area, said distribution ratio being a proportion of said diffusion layers that are distributed in said element formation area of said semiconductor device.

22. (New) A method according to claim 19, wherein said at least one fill cell includes a plurality of types of fill cells having different sizes,

wherein each of said plurality of types of fill cells having said different sizes is identified by an identifier having a same amount of information, and

wherein said arranging comprises:

arranging said plurality of types of fill cells in said vacant area in order of size, starting from a largest fill cell.

23. (New) A method according to claim 19, wherein said arranging comprises:

arranging at least one fill cell, which includes a diffusion layer and no wiring, in one of said detected vacant areas in the element formation area of said semiconductor device.

24. (New) A method of producing a layout pattern of a semiconductor device, comprising:

arranging primitive cells including circuit patterns of constituent elements of said semiconductor device in an element formation area of said semiconductor device;

detecting vacant areas in the element formation area of said semiconductor device after said primitive cells associated with all constituent elements of said semiconductor device have been arranged;

combining a plurality of unit fill cells, each including a diffusion layer and no wiring, to form at least one composite fill cell having a predetermined size;

detecting at least one continuous vacant area of said vacant areas in the element formation area of said semiconductor device, which includes a same size as said predetermined size of said composite fill cell; and

arranging said composite fill cell in said continuous vacant area.

25. (New) A method according to claim 24, further comprising:

arranging at least one unit fill cell, including a diffusion layer and no wiring, in a remaining vacant area of said vacant areas after said composite fill cell is arranged.

26. (New) A method according to claim 25, further comprising:

identifying each of said composite fill cell and said unit fill cell by an identification number,

wherein each of said identification numbers includes a same amount of information.

27. (New) A method according to claim 24, wherein said at least one composite fill cell includes a plurality of composite fill cells having predetermined sizes, and

wherein said at least one continuous vacant area includes a plurality of continuous vacant areas of said vacant areas in the element formation area of said semiconductor device.

28. (New) A method according to claim 27, wherein one of said vacant areas includes a size which is different than a size of another of said vacant areas, and

wherein one of said composite fill cells includes a size which is different than a size of another of said composite fill cells.

29. (New) A method according to claim 28, wherein said arranging comprises:

determining which of said sizes of said vacant areas match said sizes of said composite fill cells; and

arranging each of said composite fill cells in a corresponding one of said vacant areas based on said matched sizes, starting with a largest size of said composite fill cells.